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Monday, October 26 2009

**THOMSON INNOVATION**

Patent/Publication: JP9307526A DIGITAL BROADCAST RECEIVER

**Bibliography****DWPI Title**

Digital broadcasting receiver that uses orthogonal frequency division multiplexing has FFT processor for converting orthogonal frequency division multiplexing signal expressed in time domain into demodulation data expressed in frequency domain

**Original Title**

DIGITAL BROADCAST RECEIVER

**Assignee/Applicant**

Standardized: MITSUBISHI ELECTRIC CORP  
 Original: MITSUBISHI ELECTRIC CORP

**Inventor**

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**Publication Date (Kind Code)**

1997-11-28 (A)

**Application Number / Date**

JP1996123408A / 1996-05-17

**Priority Number / Date / Country**

JP1996123408A / 1996-05-17 / JP

**Abstract****Abstract**

**PROBLEM TO BE SOLVED:** To correct even a frequency deviation being an integer multiple of a carrier frequency interval by refraction the result of applying a specific product sum arithmetic operation to a frequency area complex data array.

**SOLUTION:** An OFDM digital broadcast signal is given to an antenna 1, a mixer 3 uses an oscillation signal from a voltage controlled oscillator 10 to convert the signal frequency into an intermediate frequency and the signal is demodulated into an in-phase and an orthogonal phase signal component by a quadrature demodulator 5, they are given to a FFT processing unit 7, in which they are processed into complex data in a frequency region and the result is outputted to a digital output terminal 9 via an error correction device 8. A phase correction device 13 applies phase correction processing to an array of frequency region complex data by suing complex data denoting a phase reference specified value and the result is fed to a product sum computing element 12. The product sum computing element 12 calculates products between elements apart by a same number before and after each concerned element and their total sum and gives the result of product sum operation to a detector 11. The detector 11 controls an oscillated frequency of a voltage controlled oscillator 10 so that a maximum value of the product sum operation appears at a prescribed element position of the phase reference specified value array.

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**Classes/Indexing****IPC**

IPC Code(1-7) **H04J 11/00** H04L 27/22  
 (6)

| Current IPC-R | Invention                             | Version                          | Additional | Version |
|---------------|---------------------------------------|----------------------------------|------------|---------|
| Advanced      | H04L 27/22<br>H04H 1/00<br>H04J 11/00 | 20060101<br>20060101<br>20060101 | -          | -       |

|          |   |  |   |   |
|----------|---|--|---|---|
|          | H04L 27/26  | 20060101                                     |   |   |
| Core     | H04L 27/22<br>H04H 1/00<br>H04J 11/00<br>H04L 27/26 | 20060101<br>20060101<br>20060101<br>20060101 | - | - |
| Subclass | -   | -  | - | - |

**ECLA**

H04L002726M5C3

**DWPI Manual Codes** Expand DWPI Manual Codes**Legal Status****INPADOC Legal Status**

Get Family Legal Status

**Family****Family** Expand INPADOC Family (6)**Claims**

No Claims exist for this Record

**Description****Drawing Description** Expand Drawing Description**Description** Expand Description**Citations****Citation** Expand Citing Patents (4)

Cited Patents (0)

Cited Non-patents (0)

**Other**

No Other exists for this Record

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**JP9307526A Patent Images**

Image 1 of 1

